REMARKS

Claims 26 and 33 are amended. Claims 38-47 are canceled. Claims 48-53 are added. Claims 26-37 and 48-53 are in the application for consideration.

The title has been amended, and acceptance thereof is requested.

The undersigned notes there has been no prior art or other rejection stated in the Action with respect to claim 33. Accordingly any next non-allowing Action by the Patent Office should not be made Final. Regardless, the application as presented is seen to be allowable over the references of record.

Specifically, independent claim 26 stands rejected as being anticipated by Lane et al. The Examiner is mistaken. The Examiner erroneously asserts that the opening 46 formed in Lane et al.'s insulative layer 44 is apparently the same as or equivalent to Applicant's stated well. This is error. Specifically, each of Applicant's independent claims 26 and 33 clearly are limited in requiring that a plurality of memory cell storage capacitors are received within the stated well. By way of example only, Applicant's figures depict two memory cell storage capacitors received within its depicted well 34, which is a plurality. Independent claims 26 and 33 are amended for clarification to recite a plurality of memory cell storage capacitors received within the stated one well over the word lines. The amendments do not in any way further limit or narrow independent claims 26 and 33 as such were last presented, as such limitation was already inherent in such claims as originally submitted. In Lane et al., only a single capacitor is formed within its opening 46, as is clearly depicted in Fig. 14. For Lane et al.'s opening 46 to be considered the same as or equivalent to Applicant's claimed

well, such would as a minimum require a plurality of capacitors to be formed therein, and Lane et al. clearly only shows a single capacitor formed within its opening 46.

Further, each of claims 26 and 38 are limited by their recited well peripherally defining an outline of a memory array area. A memory array area by definition will include multiple memory cells. Opening 46 in Lane et al. clearly does not define an outline of a memory array area, contrary to the Examiner assertion that it does. The Examiner is clearly mistaken in this regard and the only reasonable interpretation to a person of skill in the art is that none of the individual openings formed within Lane et al.'s structure can in any way reasonably be construed as being the same as or equivalent to Applicant's claim recited well. Accordingly, the Examiner's rejection of independent claim 26 is fundamentally in error, and any anticipation or obviousness rejection of claim 26 or claim 23 over Lane et al. would be improper. Applicant clearly recites in independent claims 26 and 33 something which is neither shown nor suggested within Lane et al., or any of the other references of record. Accordingly, formal allowance of independent claims 26 and 33 is warranted, and requested.

Dependent claims 48-53 are added, and are clearly supported in the specification at p.7, ln.21 - p.8, ln.3.

Each of Applicant's dependent claims should be allowed as depending from allowable base claims, and for their own recited features which are neither shown nor suggested in the cited art. Action to that end is requested.

The undersigned notes that an Information Disclosure Statement was filed on June 11, 2002 and the undersigned has yet to received an initialed 1449 indicating that such Disclosure Statement was considered. Consideration of the references as properly submitted is requested, and that the undersigned be provided with a copy of an appropriately initialed 1449. Further, another Supplemental Information Disclosure Statement is submitted herewith. The claims are seen to be allowable over all references of record.

This application is believed to be in immediate condition for allowance, and action to that end is requested.

Respectfully submitted,

Dated: 9-9-02

By: _____
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/810,595
Filing Date ..... March 15, 2001
Inventor ..... Belford T. Coursey
Assignee ..... Micron Technology, Inc.
Group Art Unit 2813
Examiner ..... Yennhu B. Huynh
Attorney's Docket No. MI22-1660
Title: Memory Circuitry With Array Area And Peripheral Area (As amended)

VERSION WITH MARKINGS TO SHOW CHANGES MADE ACCOMPANYING RESPONSE TO JULY 1, 2002 OFFICE ACTION

In the Title

The title is amended as follows, underlines indicate insertions and ~~strikeouts~~ indicate deletions.

Memory Circuitry With Array Area And Peripheral Area

In th Claims

The claims have been amended as follows. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

26. (Amended) Memory circuitry comprising:

a semiconductor substrate;

a plurality of word lines received over the semiconductor substrate;

an insulative layer received over the word lines and the substrate, the insulative layer having at least one well formed therein, the well comprising a base received over the word lines, the well peripherally defining an outline of a memory array area, area peripheral to the well comprising memory peripheral circuitry area;

a plurality of memory cell storage capacitors received within the one well over the word lines; and

peripheral circuitry within the peripheral circuitry area operatively configured to write to and read from the memory array.

33. (Amended) Memory circuitry comprising:

a semiconductor substrate;

an insulative layer received over the substrate, the insulative layer having at least one well formed therein, the well peripherally defining an outline of a memory array area, area peripheral to the well comprising memory peripheral circuitry area, the well having a substantially planar base;

a plurality of memory cell storage capacitors received within the one well, the memory cell storage capacitors respectively comprising a storage node container which is received partially within the insulative layer through the well base; and

peripheral circuitry within the peripheral circuitry area operatively configured to write to and read from the memory array.

Cancel claims 38-47.

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